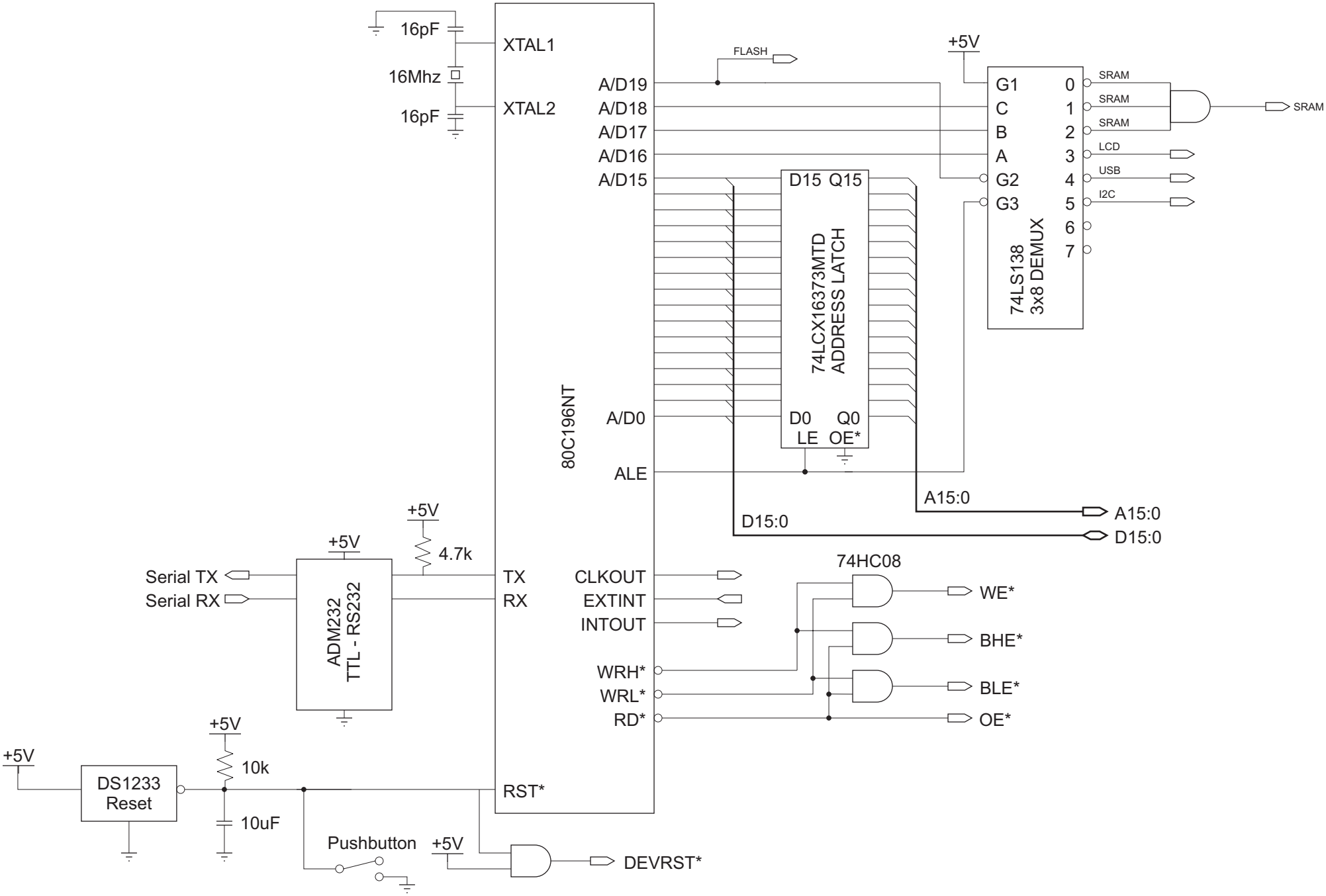
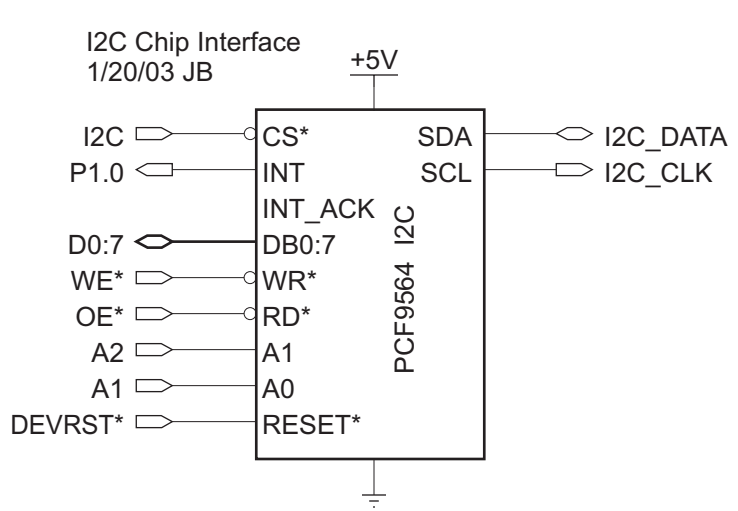
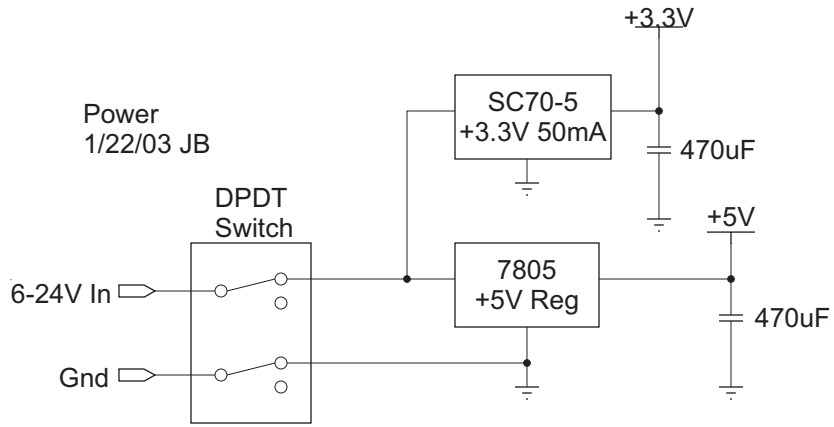
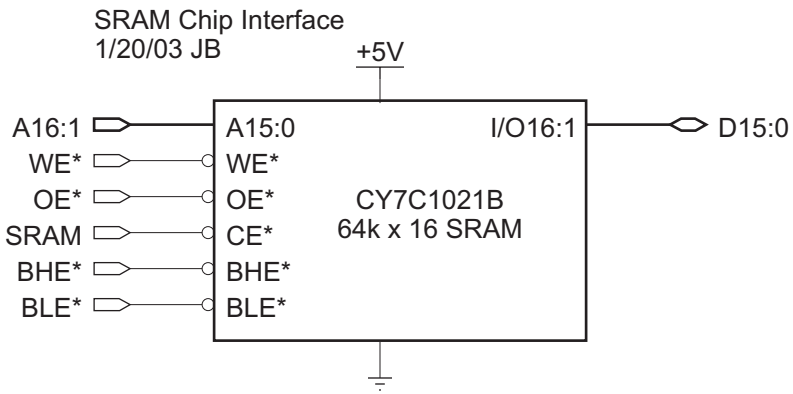
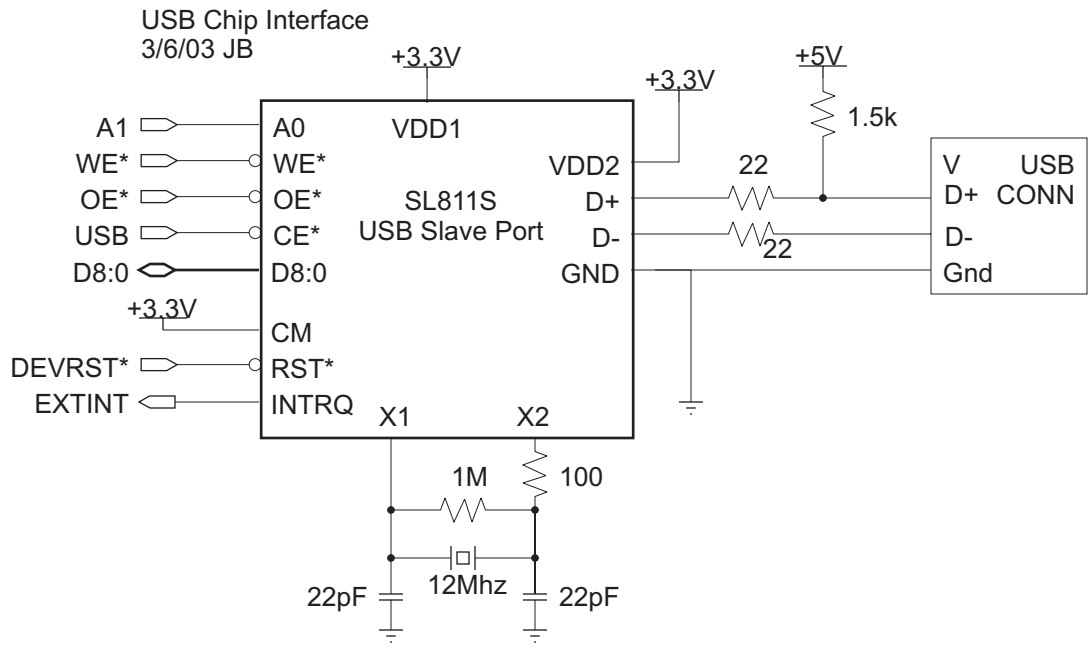
CPU/Core Bus
1/22/03 JB

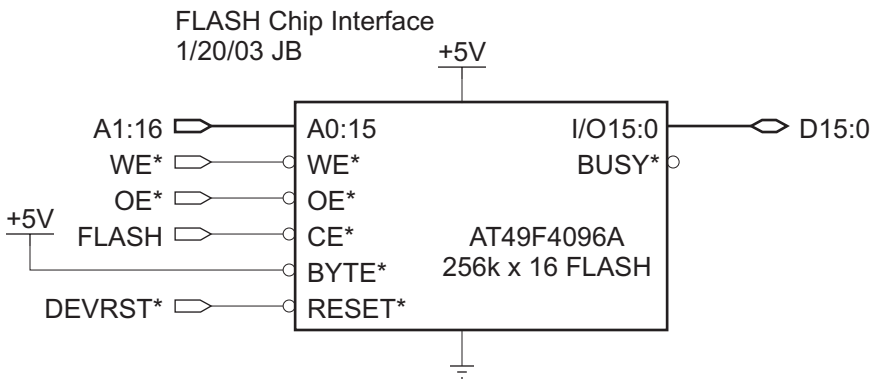



I2C Chip Interface
1/20/03 JB
+5V
I2C
P1.0
D0:7
WE*
OE*
A2
A1
DEVRST*
CS*
INT
INT_ACK
DB0:7
WR*
RD*
A1
A0
RESET*
SDA
SCL
PCF9564 I2C
I2C_DATA
I2C_CLK


Power
1/22/03 JB
+3.3V
SC70-5
+3.3V 50mA
470uF
DPDT
Switch
+5V
6-24V In
7805
+5V Reg
470uF
Gnd


SRAM Chip Interface
1/20/03 JB
+5V
A16:1
WE*
OE*
SRAM
BHE*
BLE*
A15:0
WE*
OE*
CE*
BHE*
BLE*
I/O16:1
CY7C1021B
64k x 16 SRAM
D15:0


USB Chip Interface
3/6/03 JB
+3.3V
+3.3V
+5V
1.5k
A1
WE*
OE*
USB
D8:0
+3.3V
DEVRST*
EXTINT
A0
WE*
OE*
CE*
D8:0
CM
RST*
INTRQ
VDD1
SL811S
USB Slave Port
VDD2
D+
D-
GND
22
22
V
D+
D-
Gnd
USB
CONN
X1
X2
1M
100
12Mhz
22pF
22pF


FLASH Chip Interface
1/20/03 JB
+5V
A1:16
WE*
OE*
+5V
FLASH
DEVRST*
A0:15
WE*
OE*
CE*
BYTE*
RESET*
I/O15:0
BUSY*
AT49F4096A
256k x 16 FLASH
D15:0